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ORIGINAL RESEARCH

Variations-tolerant low power wide fan-in OR logic domino circuit

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Abstract In this research, a novel strategy for reducing delay and power variations, and power dissipation in wide fan-in domino OR circuits with better noise immunity is proposed. Primarily, bulk-driven keeper transistor is used to decrease its own transconductance which reduces the delay and power variations, and removes the minimum threshold-voltage limitation. In addition, an arrangement named as keeper controlling network is developed for efficient controlling of keeper so that power dissipation can be reduced and noise immunity can be enhanced. As a result, the proposed domino circuit can be used in a wide range of fan-in designs. The proposed domino extensively performed against the process corner, voltage and temperature effect on fan-in (8, 16, 32, 64-bit) for OR logic implementations to check the reliability and robustness. The simulation values approve that the designed domino circuit displays about 31% and 25% reduction in variations of power and delay respectively, and 1.56 times noise immunity improvement in contrast with conventional domino. All domino circuits in this work are designed and simulated with SPECTRE simulator under the environment of Cadence Virtuoso using the 45 nm CMOS technology.

Keywords Low power VLSI circuits · Process variations · Noise immunity · High speed · Wide fan-in domino circuit

1 Introduction

Wide fan-in dynamic circuits are getting attention for high speed applications to implement the basic building blocks such as read path of modern microprocessors, resister files, arithmetic unit, DSP, flash memory, and tag comparators [1–3] etc. Dynamic circuits have higher speed and smaller chip area over static circuits [1]. Despite of these advantage, low signal integrity and Noise Immunity (NI) are two major drawbacks of dynamic circuits [4]. Therefore, keeper transistor and a static (INV) inverter are connected in a feedback loop having at dynamic node to enhance the NI and signal integrity as shown in Fig. 1 [4, 5], such a combination is called domino circuit. Domino circuits suffers from excessive Power Dissipation (PD) [6] because of the formation of feedback loop [4]. Scaling of devices is a better technique to reduce the PD [7] but scaling brings other issues as processes variations [8, 9] and speed loss [6]. The threshold voltage (V_{TH}) can be reduced to overcome the speed loss but subthreshold leakage current [10] increases exponentially at the same time in Pull Down Network (PDN) which results in increase the static PD and reduces the NI [11] as fan-in increases. The constant technology scaling contributes enhanced performance parameters but on the other hand, process and environment variations in performance parameters like delay, PD, NI etc. become a major challenge at circuit level [8, 9].

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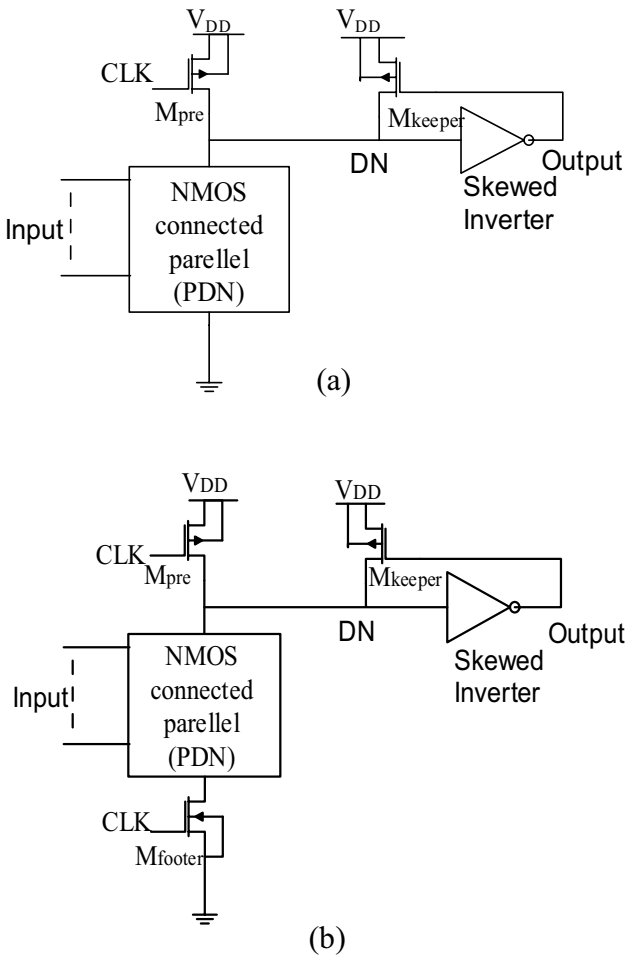

Fig. 1 CDC **a** without footer transistor, **b** with footer transistor [3, 4]

According to the nature, process variations can be categorized mainly in two kinds i.e. inter-die and intra-die. Intra-die variation generally increases sharply with technology upgrade, which degrades the performance parameters. Thus, intra-die variation is major concern for robust design implementation of wide fan-in domino OR logic circuits in nanometer technologies [12, 13]. Alioto et al. [13] have found out the effect of process variations at circuit level of abstraction. Delay and power variability in domino circuit is almost double of dynamic circuit (without feedback) because of feedback loop. Thus, process variations, subthreshold leakage current as well as NI are key alarm for the design of variation and noise tolerant low power domino circuit for wide fan-in.

In Conventional Domino Circuit (CDC) [4] as shown in Fig. 1, the stored charge in output capacitor is considered as the output logic. The CDC [4] consists a precharge transistor, an evaluation network and a feedback loop to preserve the truthful logic at dynamic node [14, 15]. The PD in domino circuit is measured with the help of mathematical Eq. (1) [16, 18];

$$P_{avg} = P_{switching} + P_{short-ckt} + P_{leakage} \tag{1}$$

where, $P_{switching}$, P_{short}, and $P_{leakage}$ is PD due to charging and discharging of output node, PD for a direct (short) path established between supply voltage (V_{dd}) and ground, and PD because of the leakage current within the devices respectively [7]. In today's scenario, leakage currents in the MOS are increasing rapidly due to the scaling of the devices. Subthreshold leakage current is a leading concern compared to all leakage components in domino because it has large amount of the total leakage current, as given in Eq. (2) [14–23];

$$I_{sub-th} = I_0\left(1 - e^{\frac{-V_{ds}}{V_{th}}}\right)\left(e^{\frac{-V_{gs}-V_{th}-\eta V_{ds}}{\eta V_{t0}}}\right), \tag{2}$$

where V_{gs}, V_{ds}, V_{th}, V_{t0}, η, n, I_0, μ_0, and C_{ox} are voltages from gate (G) to source (S), drain (D) to source (S), threshold voltage, thermal voltage, DIBL coefficient, subthreshold swing coefficient, reverse saturation current, transistor mobility at zero (0) biasing, and oxide capacitance, respectively.

Keeper transistor and evaluation transistor plays a major role to control the process variations [1, 24–34] and NI [14–23]. As a result, the most impacted relationship between keeper and evaluation transistors is characterised by the Keeper Ratio (KR), as shown in Eq. (3) [1, 14–34];

$$\mathrm{KR} = \frac{\mu_p\left(\frac{W}{L}\right)_{keeper}}{\mu_n\left(\frac{W}{L}\right)_{evalution}} \tag{3}$$

where hole and electron mobility is defined as μ_p and μ_n respectively. The ratio of (transistor size) width to length is known as W/L.

Many domino circuits are redesigned and proposed in previous studies to overcome these problems. In which, Refs. [14–23] have improved NI and reduced Power Delay Product (PDP). However, performance of these reported domino circuits is inadequate by virtue of excess or at least same delay and power variations compared to CDC [4]. On the other hand, Refs. [1, 24–34] are oriented to decrease the delay and power variations but are not capable to reduce PDP. Some domino circuits from literature work are elaborated in tabulated form to perform meta-analysis of available work and establish ground for proposed work.

Ref.	Circuit name	Methodology and outcomes	Limitations
[20]	High Speed Domino Circuit (HSDC)	• Keeper transistor is controlled efficiently in precharge and evaluation phase to reduce the dynamic PD and to improve the NI • HSD resolves the tradeoff between performance and reliability using multi-threshold voltage concept	• HSDC suffers of high delay variations as fan-in increases • It also lacks because of the drawback of pass transistor, which is used to transfer output logic to gate terminal of keeper transistor
[21]	Leakage Controlled Replica Domino Circuit (LCRDC)	• Keeper transistor is controlled by a reference analog mirror to track all process corners • Moreover, sizing of mirror transistor is done in efficient way that subthreshold leakage current might be minimized	• It is very difficult to size the mirror transistor • In case of high fan-in, it is found that leakage current and the static PD are exorbitant
[22]	Voltage Comparison based Domino Circuit (VCDC)	• Subthreshold leakage is turned down by isolating the output node to the dynamic node • Further, sensor network is added to decide the output logic based on voltages across PDN resulting a significant reduction in PDP	• The gate of transistor M4 is floating in the evaluation phase which decreases the NI • M6 is used only to increase the stacking effect, thus area and PD increase
[23]	Low Power Dynamic Circuit (LPDC)	• PD is dropped by decreasing the voltage swing of dynamic node • Further, a reference inverter is integrated in evaluation network to control the switching of footer transistor to reduce subthreshold leakage	• It is having low NI and high process variations due to reduction of voltage swing at DN • Speed is also scaled down a result of stacking effect in discharging path
[29]	Variable Threshold Voltage Keeper domino circuit (VTVKC)	• Subthreshold leakage and variations in delay and power are reduced simultaneously in this design • The threshold voltage of keeper is varied according the working phase to scale down the variations	• It is limited due to increment in delay because of the body bias generator at a phase of clock cycle • It requires an extra power supply to vary the threshold voltage
[30]	Self-Calibrating Process Compensating Dynamic circuit (PCDC)	• To bring down the process variations, a self-calibrating (PCD) Process Compensating Dynamic technique is proposed which restores the robustness of circuit • In worst case, keeper strength can also be adjusted to minimize the leakage	• The increased area is the negative criteria of this circuit design approach • This technique is limited because complexity

Ref.	Circuit name	Methodology and outcomes	Limitations
[1]	Variation-Tolerant Keeper Domino Circuit (VTKDC)	• The idea is to find out a graphical representation of the trade-off between NI and process variations • Therefore, a replica bias technique is used to keep circuit independent from random variations (e.g., random dopant fluctuation, temperature, voltage, leakage current etc.)	• PD dissipation is increased because of the sensor and extra keeper transistor • It suffers from large charge sharing same as in CDC [4]
[31]	Simple Approach to Reduce Delay in Domino circuit (SARDDC)	• First design to reduce its own transconductance by using source degeneration technique • Here, an extra PMOS is stacked in series with keeper transistor to reduce its own transconductance so that process variations in delay and power could be brought down effectively	• It has high switching PD due to the extra keeper transistor • It has low NI for high Fan-in
[32]	Variation- and Noise-Aware Reliable Dynamic Circuit (VNARDC)	• The Schmitt Trigger topology is incorporated in this design • This domino significantly mitigates the process variation in power and delay	• It lacks because of the area overhead • This domino circuit is not capable to reduce PDP in the case of wide fan-in
[33]	Clock Delayed Dual Keeper Domino Circuit (CDDKDC)	• An extra PMOS is stacked in series with keeper transistor, which is controlled by delayed clock pulse to develop the source degeneration phenomena • This arrangement is capable to reduce delay variability by using the source degeneration technique	• It consumes high PDP due to ineffective controlling of keeper transistor • Area and delay penalty because of extra PMOS keeper transistor
[34]	High Speed of Clock-Delayed Dual Keeper Domino Circuit (HSCD-DKDC)	• A controlled delay element is added to enable the switching of keeper transistor. This modification significantly improves the speed of the circuit • Further, variation is reduced by effective sizing of the keeper network	• It is complex because of the two different power supply • NI degrades for wide fan-in OR logic

From this review it can be observed that PDP is reduced at enhanced NI in most of domino circuits. Variations in delay and power are overcome in some of these circuits. These stated problems have not been considered simultaneously in a single domino circuit. Hence, this proposed work is designed to decrease the process variations and PDP by using the bulk-driven technique and efficient controlling of keeper transistor respectively at enhanced NI.

The paper is represented as follows: a literature review of Domino circuits and theoretical background is defined in Sects. 1 and 2. Proposed domino to decrease the delay and power variation, and PDP simultaneously at enhanced NI effectively is presented in Sect. 3. Simulation and comparison are done to confirm the performance upgradation of proposed domino other than existing domino in Sect. 4. Conclusion and applicability of this work is discussed in Sect. 5.

2 Preliminary study

- Noise Immunity:

  It is a very crucial task to measure NI in domino circuit to measure its reliability. Several design matrices have been developed to define NI. Unity Noise Gain (UNG) is considered for the measurement of NI [26–28]. The amplitude of the input source that causes the identical source at the output is equal to the (UNG) as given in Eq. (4).

$$\text{UNG} = \{ \text{Vnoise} : \text{Vnoise} = \text{Vout} \} \tag{4}$$

  Here, noise pulse is taken very much like the actual noise pulse in terms of glitches, ground bounce, and crosstalk etc. Generally, duration and amplitude are varied to change the level of noise pulse. However, amplitude is considered in this work.

- Figure of Merit:

  Another important performance criterion used to assess the proposed domino circuit is the Figure of Merit (FOM) [19]. Which is represented by the ratio of UNG to the product of PD, delay, and area as given in Eq. (5). All components are normalized by CDC [4].

$$FOM = \frac{\text{UNG}_{\text{norm}}}{\text{PD}_{\text{norm}} \times Delay_{norm} \times Area_{norm}} \tag{5}$$

  Temperature, frequency, supply voltage, and technology are other parameters, which may alter to FOM.

- Process variation in Domino

  To propose a wide fan-in domino circuit that decreases the delay and power variations, it is necessary to read out the concept of feedback factor for the loop formation by static INV and keeper transistor in CDC [4] as provided in Fig. 2. From [13] and [31], it is proved that delay and power variations in domino circuit are mainly because of feedback loop. Thus, mathematical expression of feedback factor is obtained to understand the method of reduction variations in domino circuit as given in Eqs. (6) and (7).

$$\text{T} = (A_{Inv} * G_{mk} * Z_{DN}) \tag{6}$$

$$\text{S} = 1/(1 - \text{T}) \tag{7}$$

  where, A_{Inv}, G_{mk}, and Z_{DN} represents the gain of static INV, keeper transistor's transconductance, and intrinsic load at the dynamic node respectively.

  As in the starting of evaluation phase , A_{Inv} is less than one, because voltages at dynamic and output node is equal to 'V_{DD}' and '0' V respectively [31]. And at the same time , G_{mk} is also less than unity because keeper transistor is in linear region. Therefore, total loop gain (T) is found less than unity as well as positive as given in Eq. (6). Equation (7) suggests the relation between closed loop gain sensitivity to variations as per the basics of control system [35]. S goes toward infinite as T approaches to unity, which means highly sensitive toward the variations. S goes toward unity as T approaches to zero, which means reduction in process variations. Therefore, it can be concluded that loop gain must decrease to overcome the delay and power variations.

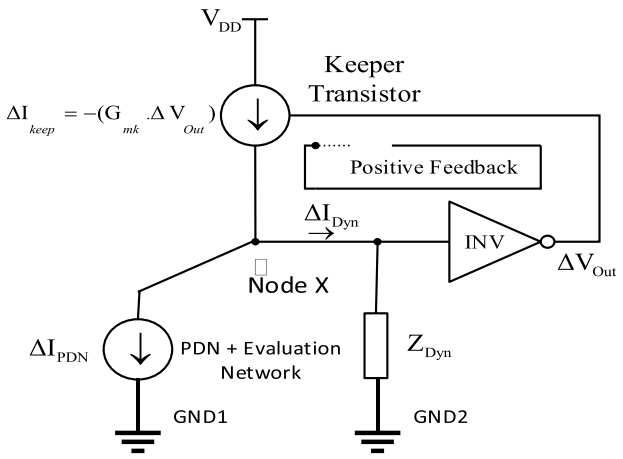

Fig. 2 Analysis of CDC [4] in current form

Since loop gain is directly proportional to the A_{inv}, G_{mk}, and Z_{DN}. Thus, loop gain can be lowered in same proportion by lowering any one of these components. As, it is very hard to control the A_{inv} and Z_{Dyn} due to their own limitation [33]. Thus, G_{mk} is reduced in the work to decrease the delay and power variations although other parameters like PD and delay etc. remain intact.

- Bulk-Driven MOS

Since, keeper transistor is used in a bulk-driven configuration (keeper transistor operates by the bulk control rather the gate control). The operation of bulk driven MOSFET is like depletion type MOSFET [36]. Primarily, gate voltage (V_{DC}) is fixed just below the threshold voltage of keeper transistor so that depletion layer is developed whereas drain current has not started to flow so far. A voltage is applied to the bulk (body) terminal of transistor to modulate drain current through transistor [36, 37]. Small signal schematic of keeper transistor using bulk-driven technique is shown in Fig. 3 and drain current is represented by Eqs. (8) and (9) respectively.

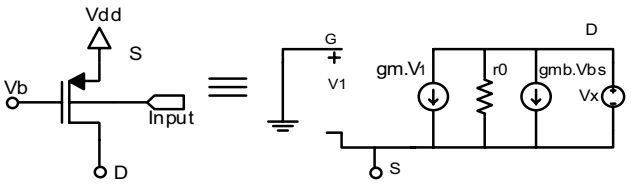

Fig. 3 Small signal schematic of Bulk-driven Keeper Transistor

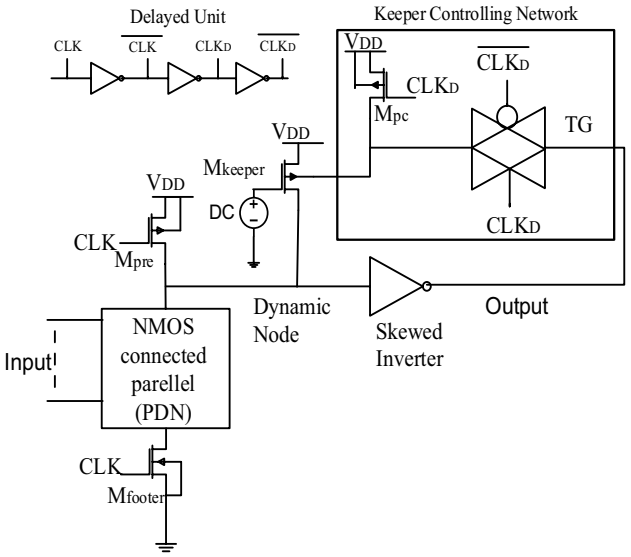

Fig. 4 Schematic representation of proposed domino circuit

$$I_d = \frac{K'W}{L}\left(V_{gs} - V_{t0} - \gamma\left(\sqrt{2\phi_f - V_{bs}} + \sqrt{2\phi_f}\right) - \frac{n}{2}V_{ds}\right) \quad V_{ds}, V_{ds} < V_{ds}(sat) \tag{8}$$

$$I_d = \frac{K \cdot W}{L}\left(V_{gs} - V_{t0} - \gamma\left(\sqrt{2\phi_f - V_{bs}} + \sqrt{2\phi_f}\right)\right)^2, \quad V_{ds} > V_{ds}(sat) \tag{9}$$

$$G_{mbk} = \frac{dI_d}{dV_{bs}} = \frac{\gamma G_{mk}}{2\sqrt{2\phi_f - V_{bs}}} = \eta\, G_{mk} \tag{10}$$

where K', γ, and ϕ_f represents transconductance parameter, substrate-bias (body-effect) coefficient, and fermi potential. G_{mbk} and G_{mk} are the transconductance of keeper transistor for bulk-driven technique and gate-driven technique respectively. However, η is the ratio of G_{mbk} to G_{mk}. Range of coefficient depends on the technology node, which is 0.2–0.4 for below 90 nm channel length [38]. Therefore, it can be said as per the Eq. (10) that transconductance of keeper under bulk-driven technique is less than gate-driven [39] technique.

3 Proposed domino

The proposed domino circuit as depicted in Fig. 4 is designed using bulk driven technique. This technique minimizes significantly the delay and power variations and enhances the NI. However, PD is somewhat increased because of the developed depletion layer. To manage the switching behavior of the keeper transistor, an effective combination of transistors known as the keeper controlling network is implemented, which minimizes the PD. This arrangement improves the NI also.

The bulk driven technique provides low transconductance and no threshold voltage limitation over a gate-driven device. As per Eq. (10), transconductance of bulk-driven keeper is substantially reduced from 0.2 to 0.4 times than the gate-driven transconductance [36, 38] which consequently reduces loop gain factor (T) in same proportion. This reduction in loop gain factor significantly decreases the delay and power variations. Thus, reduced transconductance will boost the robustness of the domino circuit against the variations. Further, it is worth noting here that threshold voltage constraint vanishes, and transistor responds for both positive and negative bias voltages (V_{bs}) just because of the developed depletion layer due to V_{DC} [37]. A small voltage (at the output node) provided to the body of the keeper transistor, is sufficient to turn it on and quickly charge the dynamic node to V_{dd}. In addition, a single keeper transistor having minimum size can keep dynamic node at truthful logic in the case of large fan-in. Furthermore, this minimum size is advantageous to keep the PD and variations minimum because transconductance of transistor is directly proportional to its own width. Now, dynamic node will fully charge and discharge properly which maximizes dynamic range of the domino circuit. Therefore, both characteristics of bulk driven i.e. low transconductance and no threshold voltage limitation are beneficial for domino circuit.

Furthermore, an extension of HSD [22] is incorporated for efficient controlling of keeper transistor in the proposed domino circuit in order to minimize PDP and enhance NI. In this arrangement (keeper controlling network), output node and supply voltage are connected to body terminal of keeper transistor through a Transmission Gate (TG) and PMOS transistor (M_{pc}) respectively. Transistor M_{pc} is used to turn OFF the keeper transistor in precharge phase which significantly reduces dynamic PD. Moreover, TG is used in place of pass transistor in proposed domino because it transfers the full 'V_{dd}' and '0' voltage without any degradation [40] so that keeper transistor can be completely turned ON and OFF. Also, the lower ON resistance of TG reduces the overall delay of domino circuit effectively [40]. Thus, TG is used to transfer the exact output logic with high switching speed to the body of keeper transistor in evaluation phase,

which quickly turns ON and OFF the keeper transistor in order to fully charge and discharge the dynamic node.

In the case of wide fan-in OR logic, unwanted discharging of dynamic node is increased by subthreshold leakage current. Therefore, bulk-driven keeper transistor is used in evaluation phase to re-charge the dynamic node with an efficient controlling and high speed, whereas footer transistor is incorporated to avoid any leakage during precharge phase. Thus, both dynamic and output nodes are fully shielded by noise and unnecessary charge sharing. Consequently, NI is enhanced along with reduced PDP in the proposed domino.

Both phases of the proposed domino circuit's operation are described in detail below, similar to CDC [4];

- Precharge Phase:
  In this phase, clock (CLK) and $\overline{CLK}$ are at logic '0' and '1' (V_{dd}) and all given input are at logic '0'. Thus, all transistors in PDN including footer transistor are turned OFF, and transistors M_{pre} turns ON which charges the dynamic node upto logic high which discharges the output node through low-skewed inverter. After certain delay, M_{pc} and TG turn ON and OFF respectively resulting in a high voltage being applied to bulk of keeper transistor. Therefore, keeper transistor is turned OFF. Further, transistor M_{footer} is turned OFF to avoid any unnecessary discharging of dynamic node. At the end of this phase, the logic of the dynamic and output nodes are '1' and '0,' respectively.
- Evaluation Phase:
  In the starting of this phase, clock (CLK) and $\overline{CLK}$ are at the logic '1' (V_{dd}) and '0' consequently transistors M_{pre} and footer turn OFF and ON respectively. After certain delay, M_{pc} and TG are turned OFF and ON respectively. Since, TG is ON due to which output node is directly connected to body of keeper. Thus, keeper will be controlled by output node. Now, dynamic node may discharge or re-charge depending on the transistors of PDN. Therefore, next phase of evaluation phase will depend on applying inputs to transistors of PDN (NMOS connected in parallel), which may either be '1' or '0'.

Now, two case can occur. In first case, all inputs are at logic '0' resulting all parallel transistors in PDN to turn OFF which signifies logic high and low at dynamic and output nodes respectively. Thus, logic low will be applied to the body of keeper transistor because TG is ON. Due to which keeper starts to re-charge the dynamic node if any discharging occurs because of subthreshold leakage current. Hence, dynamic and output nodes will stay at logic high '1' and low '0' respectively.

In second case, at least one input should be at high logic resulting at least one PDN transistor to be turned ON. As a result, dynamic nodes have access to at least one discharging path, and dynamic node begin to discharge through that way. As a result, the output capacitor begins to charge through a low skewed inverter. Further, output node becomes at logic '1' which completely turns OFF the keeper transistor. Finally, the logic '0' and '1' appear to the dynamic and output nodes, respectively. The output waveform is obtained by simulating the proposed domino to verify the 32-bit OR logic as given in Fig. 5.

4 Results and comparison of simulation

All the circuits are designed and simulated under the same environment using SPECTRE simulator in Cadence Virtuoso tool to observe the performance parameters and verify the results so that a fair discussion can be done. Initially, temperature, power supply, frequency and output load are considered to be at room temperature, 1 V, 1Ghz, and 5fF during simulation respectively. These simulation values are varied to consider all the environment effects on the proposed circuits. The performance constraints of the proposed circuit are evaluated for different fan-in; 8, 16, 32, 64-input under worst case delay. A framework, which is setup by Alioto et al. [13] is taken to obtain all the performance specifications given in Fig. 6.

Average normalized PD and UNG for previously reported circuits and proposed domino circuit are attained at different fan-in as presented in Table 1. This table depicts that PD is reduced by 18–37% in the proposed domino with respect to CDC [4]. This table also illustrates that NI of the proposed domino is improved by 1.43–1.56 times as compared to the CDC [4]. Because of the efficient controlling of the keeper transistor PD has been reduced and improvement in NI is due to the bulk driven technique which vanishes the minimum voltage requirement. Moreover, dynamic node is efficiently charged and discharged because of the controlled keeper transistor. Therefore, proposed domino circuit shows reduction in PD and improved NI in contrast to previously reported domino circuits.

With the use of Eq. (5), the FOM values for all previously reported and proposed domino circuits are computed and illustrated at 32-bit fan-in by a bar-chart in Fig. 7. CDC [4] normalizes the value of FOM for each domino circuit to easily see the improvement in proposed domino circuits compared to previously reported domino circuits. Predicted area is simply obtained by transistor count of designed circuit, which is used to calculate the FOM. Since, area of PMOS is nearly twice than NMOS therefore single PMOS is taken on two NMOS count. With a comparison of FOM through Fig. 7, the proposed domino has a greater FOM than other existing reported domino circuits.

Table 1 Comparative analysis of normalized values of PD and UNG at different fan-in among proposed domino and keeping similar delay

Fan-in	Existing domino	CDC [4]	HSDC [20]	LCRDC [21]	LPDC [23]	VTVKC [29]	VTKDC [1]	SARDDC [31]	VNRDC [32]	HSCDDKDC [34]	Proposed domino
8-bit (60pS)	Normalized PD	1.00	0.90	0.77	0.85	0.99	0.92	0.83	0.96	0.89	0.82
	Normalized UNG	1.00	1.17	1.07	1.30	1.27	1.10	1.20	1.27	1.23	1.43
16-bit (70pS)	Normalized PD	1.00	0.88	0.85	0.91	0.98	0.93	0.78	0.95	0.91	0.75
	Normalized UNG	1.00	1.19	1.07	1.30	1.26	1.15	1.19	1.33	1.26	1.44
32-bit (80pS)	Normalized PD	1.00	0.97	0.73	0.79	0.92	0.89	0.74	0.87	0.82	0.66
	Normalized UNG	1.00	1.17	1.04	1.30	1.35	1.13	1.17	1.35	1.26	1.48
64-bit (90pS)	Normalized PD	1.00	0.95	0.72	0.73	0.87	0.82	0.82	0.90	0.78	0.63
	Normalized UNG	1.00	1.11	1.00	1.28	1.28	1.06	1.11	1.33	1.22	1.56

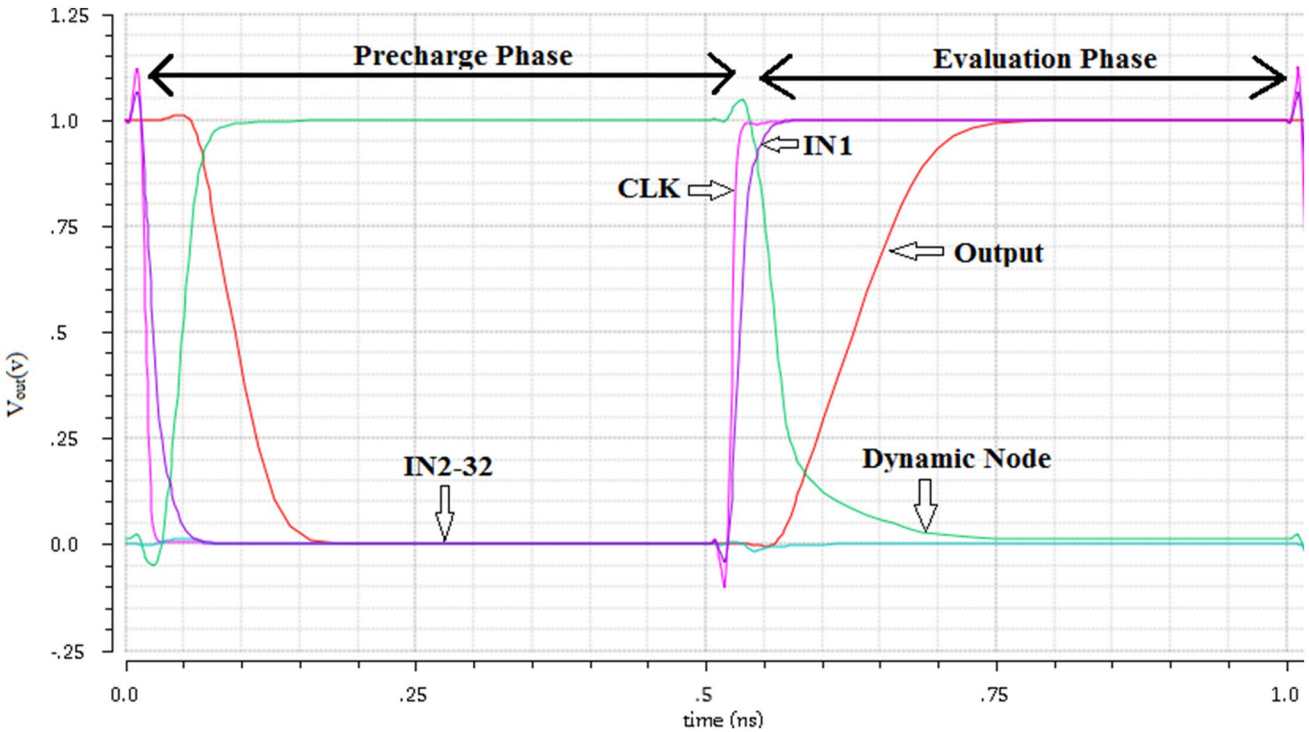

Fig. 5 Simulated output waveform for the proposed domino circuit at 32-bit fan-in OR gate

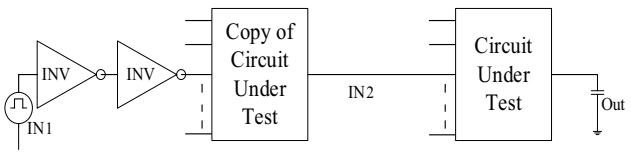

Fig. 6 Simulation setup used in this work

The most important task of the proposed domino must authenticate the circuit against process and environment variations. Therefore, proposed and previously reported domino circuits are simulated to find out the standard deviation (SD) of delay and PD at different fan-in to identify the variations reduction in delay and PD. All normalized values of SD are listed in Table 2 to compare proposed and previously cited domino. In this work, Monte Carlo simulation at 2000 iterations is performed to find out the effect of process variations with 2000 iterations so that highly accurate results can be obtained as in [31]. Table 2 shows 25% reduction in SD of PD and 31% reduction in SD of delay in proposed domino as compared to CDC [4]. Because of the keeper transistor's reduced transconductance, the delay and power variations have been reduced.

Effect of process, voltage, and temperature (PVT) variations must be included to substantiate the stability, robustness, and reliability. Thus, the proposed domino

along with some previously reported circuits are evaluated at different process corners, temperature, and voltages to take into account of the PVT effect. First, delay and power variability as well as SD are obtained at different corners, temperatures, and voltages given in Table 3, Figs. 8, 9 and 10. Table 3 describes that both delay and power variability are reduced at most of the corners in contrast to CDC [4] and SARDDC [31].

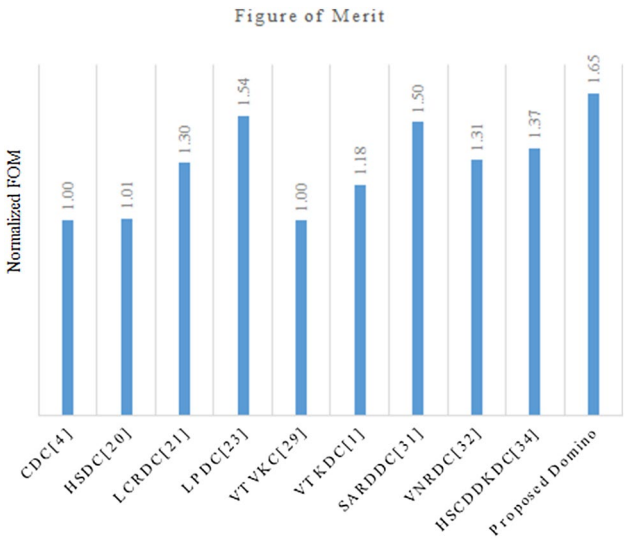

Fig. 7 Comparative analysis of the normalized FOM

Further, proposed design along with CDC [4] for 32-bit fan-in is simulated at different voltage nodes to consider the voltage variation as given in Fig. 8. All the values of PD and delay in Fig. 8 are normalized by CDC [4]. Figure 8 shows that PD for both domino circuits has increased with respect to voltage whereas delay is reduced. Because, PD directly depends on the square of V_{DD}. Moreover, PD and delay of proposed domino circuit are less than the CDC [4] at each voltage node and less fluctuating with respect to voltage.

Furthermore, the proposed domino circuit along with CDC [4] is simulated at different temperatures. Thus, numerical values of delay and PD are obtained at different temperatures. Figures 9 and 10 are plotted using these values so that a comparison could done between proposed domino and CDC [4]. It can be seen through both the Figs. 9 and 10 that delay and PD are increasing linearly for proposed domino with temperature according to the basic property of temperature increment. Whereas, both PD and delay are linearly increasing but start to decrease above 100 °C in the case of CDC [4].

Thus, it can be said that the proposed domino is more consistent and tolerant of fluctuations brought on by process and environment. Hence, it is verified through all the results of PVT effect that robustness, stability and reliability of the

Table 2 Comparative analysis of normalized (σ) standard deviation in the delay and PD at different fan-in among proposed domino and previously reported domino keeping similar delay

Fan-in	Existing domino	CDC [4]	HSDC [20]	LCRD [21]	LPDC [23]	VTVKC [29]	VTKDC [1]	SARDDC [31]	VNRDC [32]	HSCDDKDC [34]	Proposed domino
8-bit (60pS)	σ_{PD}	1.00	0.97	1.00	0.92	0.91	0.89	0.90	0.93	0.89	0.84
	σ_{Delay}	1.00	0.83	0.84	0.91	0.84	0.90	0.94	0.89	0.90	0.85
16-bit (70pS)	σ_{PD}	1.00	0.93	0.95	0.84	0.76	0.84	0.86	0.89	0.86	0.83
	σ_{Delay}	1.00	1.01	0.83	0.81	0.91	0.88	0.89	0.86	0.87	0.82
32-bit (80pS)	σ_{PD}	1.00	0.89	0.90	0.91	0.87	0.83	0.85	0.86	0.84	0.81
	σ_{Delay}	1.00	0.96	0.97	0.97	0.89	0.93	0.88	0.84	0.85	0.77
64-bit (90pS)	σ_{PD}	1.00	0.87	0.90	0.89	0.82	0.80	0.83	0.88	0.82	0.75
	σ_{Delay}	1.00	0.91	0.98	0.86	0.80	0.77	0.79	0.77	0.78	0.69

Table 3 Comparative analysis of (σ) SD and (σ/μ) processes variability in the delay and PD among the proposed, SARDDC [31] and CDC [4] at different corners keeping similar delay

Load (fF)	CDC [4]				SARDDC [31]				Proposed domino			
	PD		Delay		PD		Delay		PD		Delay	
	σ(μW)	(σ/μ)	σ(pS)	(σ/μ)	σ(μW)	(σ/μ)	σ(pS)	(σ/μ)	σ(μW)	(σ/μ)	σ(pS)	(σ/μ)
TT	0.651	0.041	8.748	0.111	0.542	0.048	5.678	0.070	0.491	0.046	4.059	0.050
FF	0.608	0.038	5.660	0.090	0.576	0.041	4.983	0.069	0.568	0.044	3.552	0.047
SS	0.588	0.038	11.330	0.107	0.302	0.029	7.256	0.072	0.268	0.029	5.038	0.051
FS	0.392	0.028	9.672	0.121	0.336	0.026	5.781	0.075	0.295	0.031	3.231	0.043
SF	0.950	0.051	12.100	0.108	0.885	0.065	9.816	0.089	0.785	0.063	8.445	0.077

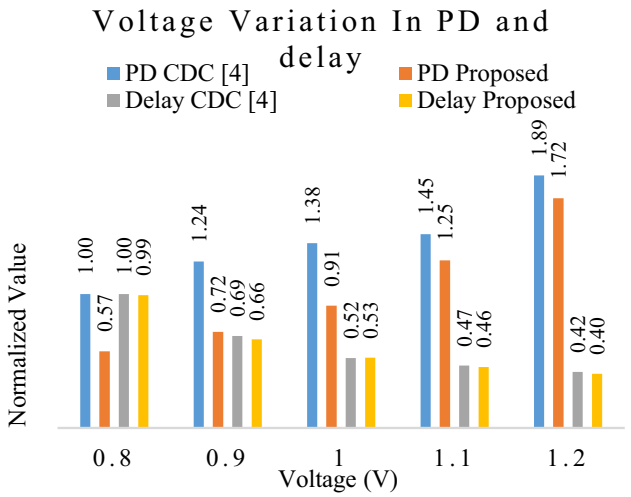

Fig. 8 Comparative analysis of voltage variation in delay and PD for the proposed domino and CDC [4]

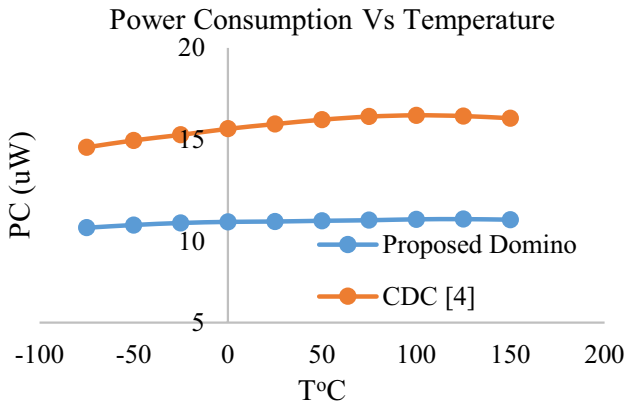

Fig. 9 Comparative analysis of Temperature variation in PD for the proposed domino and CDC [4]

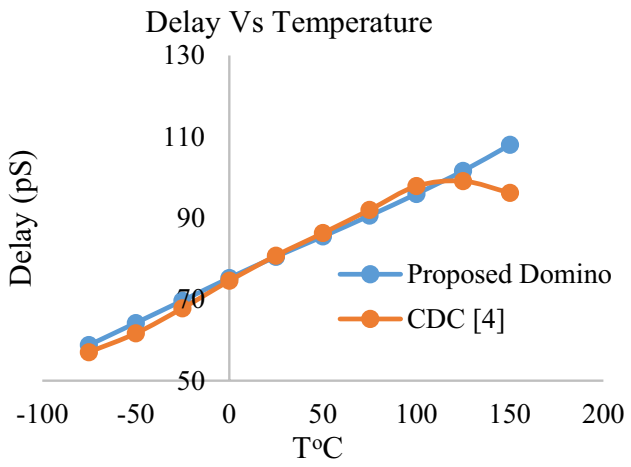

Fig. 10 Comparative analysis of Temperature variation in Delay for the proposed domino and CDC [4]

proposed domino are enhanced in contrast to the SARDDC [31] and CDC [4]. These enhancements have happened as a result of the scaling down in the transconductance of keeper transistor due to bulk-driven technique and efficient controlling of the keeper transistor.

5 Conclusion

The wide fan-in OR gate domino circuits suffer due to high process variations and subthreshold leakage current resulting degrading performances. Thus, a novel technique to decrease the delay and power variation, and PDP at improved noise immunity is presented and compared to existing domino. In which, keeper transistor is connected in bulk-driven technique to reduce the process variations by decreasing its own transconductance. Moreover, an architecture is designed for the efficient controlling of keeper so that proposed domino can offer minimal PDP and improved noise immunity. However, the use of extra transistor to design the architecture for the controlling of keeper increases total area of the novel keeper circuit. The novel keeper style minimises the delay and power variations by nearly 25% and 31%, respectively, as compared to the conventional keeper style when doing 2000 runs in Monte Carlo simulations of the ADE-XL environment. The simulations demonstrate that bulk-driven PMOS keeper transistor offers minimal variations in delay and power with good reliability and robustness compared to the gate-driven keeper.

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